TIMKEN

MPS160

Multiplying Encoder ASIC

DEVICE SPECIFICATION

Revision 2.32

12 SEP 2019

The Timken Company

AEC-Q100
Compliant
RoHS
Compliant
REACH
Compliant

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1. PROJECT SUMMARY

1.1 PURPOSE OF SPECIFICATION

The purpose of this specification is to define the mechanical, environmental and electrical characteristics for integrated circuits supplied by *Timken*. All parts that comply with this specification will be considered to meet the customer's requirements. Any parameter left undefined will be processed according to *Timken*' normal quality control standards.

Parameters defined in this document take precedence over parameters defined in applicable customer documents.

1.2 GENERAL INFORMATION

ASIC/Sensor:	ASIC/Sensor Name:	MPS160
	Package Type:	TSSOP-24
	Number of Pins:	24
Timken:	Technical Contact:	
	Telephone:	
	Email:	John.santos@timken.com
		Rob.stiffler@timken.com

2. PACKAGE AND MARKING

2.1 PIN DESCRIPTION

Pin	Pin Name	Pin Type	Special Requirements	Notes / Library Cell Name
1	PRG	DI_PD	For use by Timken only	Programming Input ; Connect to VDD during operation
2	VSS	S	Double Bond	Negative Supply
3	A	DO_OD	10 mA	Incremental quadrature position output A
4	VDDP	S	Internal connection to VDD	Positive Supply – Output Buffer Supply Support
5	B	DO_OD	10 mA	Incremental quadrature position output B
6	Test Pin 6			Used for testing – Ground during use.
7	CAO	AO	For use by Timken only	Common Analog Output for internal signals
8	VDD	S	Double Bond	Positive Supply
9	CD	DO_OD	10 mA	Incremental Reference Position Outputs C and D
10	DO	DO		Data Output for SSI
11	X	DI_ST_PD		X digital input
12	CLK	DI_ST		SSI Clock input
13	CSn	DI_ST		Chip Select / active low
14	PD_W	DI_ST		W digital input or Low Power Mode (PD_InpEN)
15	Test Pin 15			Used for testing – Ground during use.
16	Test Pin 16			Used for testing – Ground during use.
17	Test Pin 17			Used for testing – Ground during use.
18	VSS Coil	S	Internal connection to VSS	Used for testing – Ground during use.
19	VDD Hall	S	Internal connection to VDD	Positive Supply – Hall Bias Supply Support
20	Test Pin 20			Used for testing – Ground during use.
21	Test Pin 21			Used for testing – Ground during use.
22	Test Pin 22			Used for testing – Ground during use.
23	U	DI_ST		U digital input
24	V	DI_ST		V digital input

Table 2.1 Pin Description

PIN Types:

S	supply pad
AIO	analog I/O
AO	analog output
DI	digital input
DI_PD	digital input with pull down structure
DI_ST_	digital input with schmitt trigger
DI_ST_PD	digital input with schmitt trigger and pull down structure
DO	digital output
DO_OD	digital output open drain / push - pull
NC	Not Connected

2.2 MARKING / PACKAGE

Package type: TSSOP-24 (SIZ-X) / Lead-Free Package

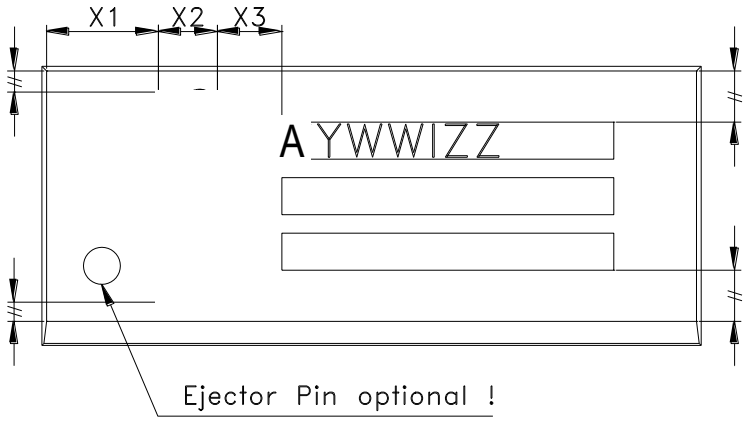


Figure 2.1 Package Marking

Marking: Lot / date codes

YYWWXZZ YY ..... Pb-free (acc. CN01-2010),
YY …….year
WW ..... week
X ..... plant identifier (M, R)
ZZ ..... lot information

Customer Marking: First Line **MPS160 (or specific programming variant code)**
Second Line **B**

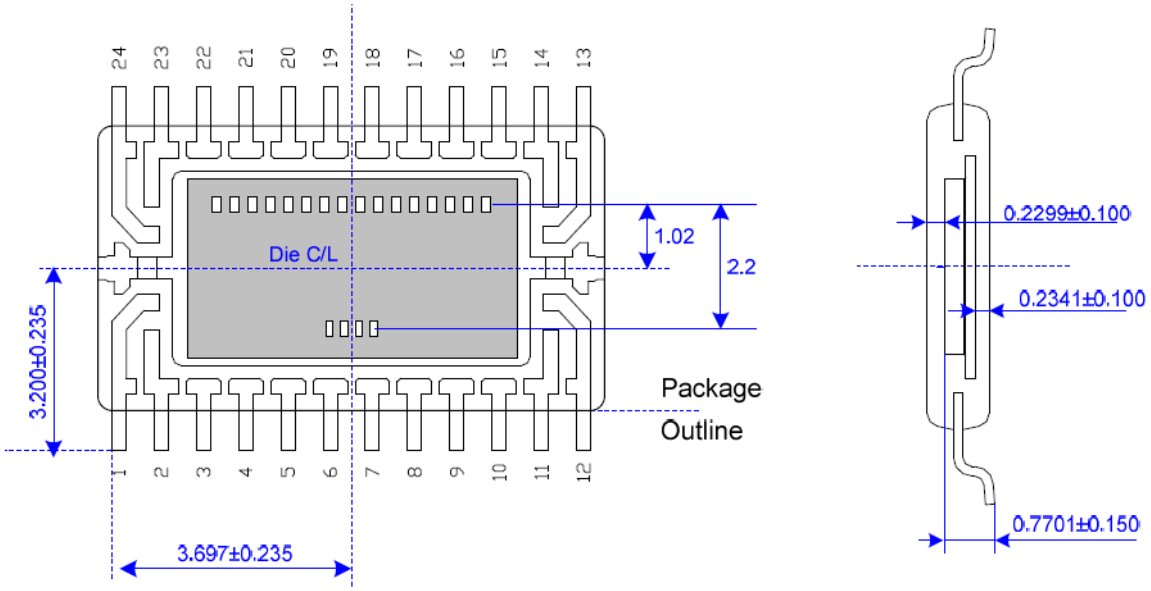


Figure 2.2 Die in Package (TSSOP-24)

3. GENERAL DEVICE SPECIFICATIONS

3.1 ABSOLUTE MAXIMUM RATINGS (NON OPERATING)

Stresses beyond those listed under “Absolute Maximum Ratings“ may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under “Operating Conditions” is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Parameter	Symbol	Min	Max	Unit	Note
Analog Supply Voltage	AVDD	-0.3	7	V	
Digital Supply Voltage	DVDD				
Input Pin Voltage	V_{in}	VSS – 0.5	VDD + 0.5	V	
Input Current (latchup immunity)	I_{scr}	-100	100	mA	Norm: Jedec 17
Electrostatic Discharge	ESD		± 2	kV	Norm: MIL 883 E method 3015
Pkg. Thermal Resistance TSSOP-24	Θ_{JA}		58.3	°C / W	Multi-Layer PCB
Pkg. Thermal Resistance EP-TSSOP-24	Θ_{JA-EP}		38	°C / W	Multi-Layer PCB
Storage Temperature	T_{strg}	-55	175	°C	According AMKOR datasheet
Package body temperature	T_{body}		260	°C	Norm: IPC/JEDEC J-STD-020C (1) (2)
Humidity non-condensing		5	85	%	

Table 3.1 Absolute Maximum Ratings

(1) The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020C “Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices”.

(2) The lead finish for Pb-free leaded packages is “Matte Tin” (100% Sn).

3.2 OPERATING CONDITIONS

All in this specification defined tolerances of parameters are assured over the whole operation conditions range and also over lifetime.

Parameter	Symbol	Min	Max	Unit	Note
Positive Analog Supply Voltage	AVDD	4.5	5.5	V	Except for SPZ programming
Positive Digital Supply Voltage	DVDD				
Negative Analog Supply Voltage	AVSS	0.0	0.0	V	
Negative Digital Supply Voltage	DVSS				
Power supply current	I_{DD}		41	mA	A / B / CD / CAO unloaded
Ambient temperature	T_{amb}	– 40	125	°C	TSSOP-24 & EP-TSSOP-24
Junction temperature	T_J	– 40	150	°C	

Table 3.2 Operating Conditions

********* Timken recommends the use of a 0.01uF or a 0.1uF decoupling capacitor as near the ASIC as possible between any of the Vdd pins and Vss.**

3.3 SYSTEM PARAMETERS

Parameter	Symbol	Min	Max	Unit	Note
Power Up Time	T_{PwrUp}		500	µs	(3)
Propagation Delay	T_{prop}		20	µs	(4)

Table 3.3 System Parameters

(3) Amplitude within valid range. Interpolator locked. VDD = 4.5 V min.
(4) Time between one bit change in the Hall signal to A and B quadrature outputs.

3.4 DC/AC CHARACTERISTICS FOR DIGITAL INPUTS AND OUTPUTS

3.4.1 A / B / CD Open Drain; Push/Pull Output

Open Drain Mode programmable. Default: Push Pull Mode.

Parameter	Symbol	Min	Typ	Max	Unit	Note
High level output voltage	V_{OH}	0.8 DVDD			V	
Low level output voltage	V_{OL}			0.4 + DVSS	V	
Current source capability		8			mA	Push/Pull mode
Current sink capability	I_L	10			mA	
Short Circuit Limitation Current	I_{short}			28	mA	
Capacitive load	C_L		20		pF	
Resistive load	R_L		820		Ω	
Rise time	t_R			1.2	µs	According to MPS32x
Fall time	t_F			1.2	µs	According to MPS32x

Table 3.4 A / B / CD Open Drain Output

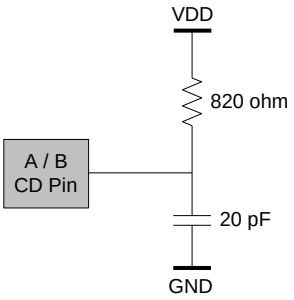


Figure 3.1 A / B / CD Open Drain Output

3.4.2 U, V, PD_W, X, CLK, CSn Digital input

Schmitt trigger input data.

Parameter	Symbol	Min	Max	Unit	Note
Negative-Going Threshold	V_{t-}	1.1	1.6	V	VDD=4.5V
		1.4	1.9	V	VDD=5.5V
Positive-Going Threshold	V_{t+}	2.8	3.2	V	VDD=4.5V
		3.4	3.9	V	VDD=5.5V

Table 3.5: Schmitt trigger input levels

3.4.3 DO Digital output

4mA tri-state digital output.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output-low voltage	V_{OL}			0.4	V	VDD=4.5V
Output-high voltage	V_{OH}	4.0			V	VDD=4.5V
Current capability	I_{OUT}			3	mA	Sink and source

Table 3.6: digital output levels

4. TECHNICAL DESCRIPTION

4.1 SHORT DESCRIPTION / KEY FEATURES

Main application of the device is contact-less, angular position detection with incremental output and Synchronous Serial Interface.

4.2 SYSTEM DIAGRAM / DESCRIPTION

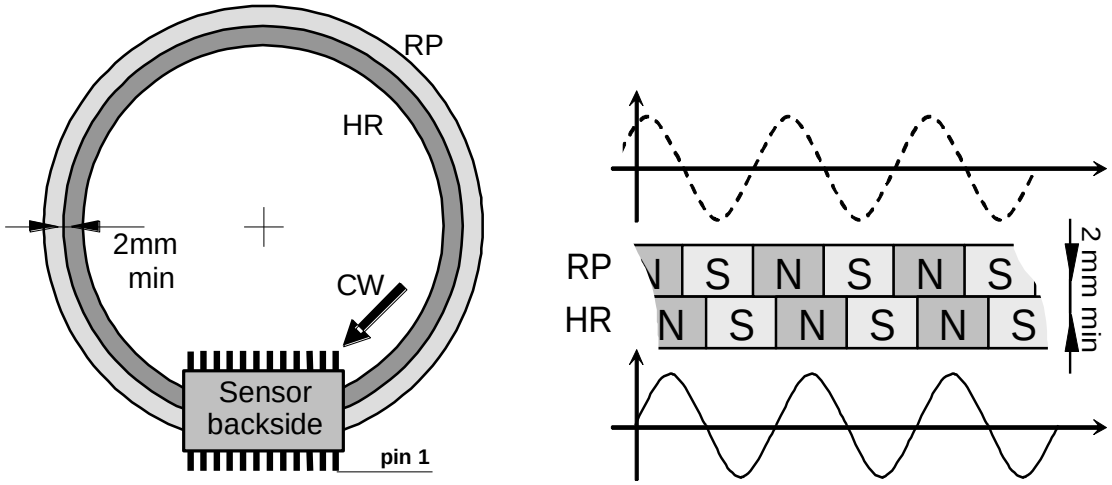


Figure 4.1 System Arrangement Encoder Ring / Sensor ASIC

A rotating encoder ring provides the input field by permanent magnetic north (N) and south (S) poles along its circumference. The ASIC Hall sensor system measures the magnetic field and converts it into an electrical signal. Up to 160 digital absolute steps within one pole pair period can be detected. A standard quadrature A / B incremental output is derived to indicate the direction of rotation and to increase the resolution of the encoder ring by a maximum multiplying factor of 40 (pulses/pole pair).

A Synchronous Serial Interface unit provides also the absolute position (angle) within one pole pair.

Additional to the high resolution incremental output, two reference signals C and D can be enabled, triggered by a magnetic singularity on a second track of the encoder ring. This allows absolute position measurements over one rotation.

The length of the sensor string is programmable. Also the interpolation factor is programmable.

An Automatic Gain Control helps to cover the demanded large dynamic input range (1:12).

Designed to reject magnetic bias fields up to +/- 15 mT

RoHS Compliant, AEC-Q100 Compliant

4.3 SYSTEM BOCK DIAGRAM

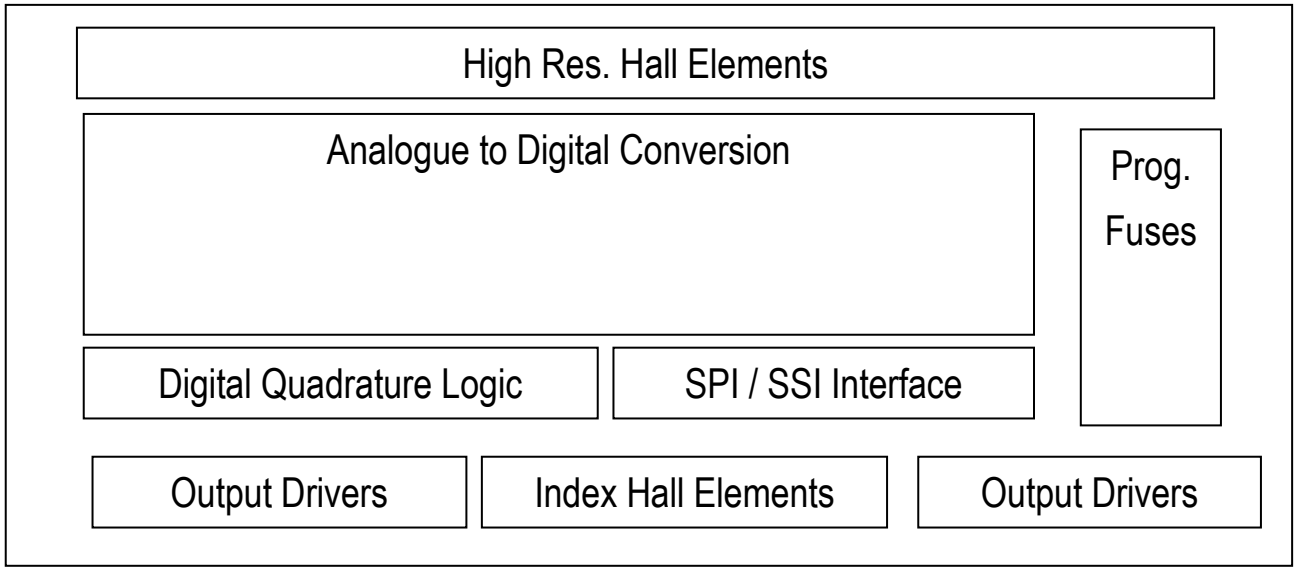


Figure 4.2 Sensor ASIC Block Diagram

5. DETAILED SYSTEM AND BLOCK SPECIFICATIONS

5.1 MAGNETIC INPUT

Sinusoidal characteristics of the magnetic Encoder Ring apply to High Resolution (HR) and Reference Pulse (RP) Track.

Parameter	Symbol	Min	Max	Unit	Note
Magnetic Pole Length (Full Period/FP)	$L_{P\text{-}FP}$	0.80	4	mm	(7)
Magnetic Period (Full Period/FP)	$T_{P\text{-}FP}$	1.6	8	mm	$T_{P\text{-}FP} = 2 \times L_{P\text{-}FP}$
Magnetic Pole Length (Half Period/HP)	$L_{P\text{-}HP}$	3.0	6.0	mm	(7)
Magnetic Period (Half Period/HP)	$T_{P\text{-}HP}$	6.0	12.0	mm	$T_{P\text{-}HP} = 2 \times L_{P\text{-}HP}$
Pole Length Relative Accuracy	P		±4	%	0
Magnetic Amplitude	A_{mag}	5	60	mT	(1) (7) (8) (9)
Operating Dynamic Input Range		1:12	1:24		(10)
Magnetic Offset	Off_{mag}		± 0.5	mT	All DP & HP modes
Amplitude Modulation	AM_{mag}		± 15	%	F_{AM_max}
Magnetic Temperature Drift	T_{dmag}		– 0.2	%/K	
Input Frequency	f_{mag}	0	5	kHz	

Table 5.1 Magnetic Input Characteristic

Two additional configurations, Double Period (DP) mode and Half Period (HP) mode can be enabled. No differential signal processing for canceling magnetic offsets on the HR for the signal is possible in HP mode.

(5) $P = (L_P – L_{P,th}) / L_{P,th}$ where $L_{P,th}$ is the theoretical pole length
(6) Absolute magnetic input minimum 5 mT over all parameters. This minimum input results into a transition noise of 2 LSB_{PP}. An increased hysteresis of 2 LSB must be chosen for no additional pulses, or the input magnetic amplitude must be doubled to 10 mT to use 1 LSB hysteresis.
(7) The magnetic input minimum amplitude increases with increasing pole length, as reported in the table below:

Pole Length [mm]	0.76 to 1.25	1.13 to 2.15	1.51 to 2.50	2.50 to 4	4 to 6
Min. Magnetic Amplitude [mT]	5	7	5	7.5	10
Mode	DP	FP	FP-A (Normal Operating Mode)	FP-B (Normal Operating Mode)	HP

Figure 5.1 Min. Magnetic Amplitude Vs. Pole Length

(8) Due to shock sudden variation of 20% are possible.
(9) The minimum magnetic field of the magnetic singularity can go down to 70% of the minimum magnetic amplitude of the HR track.
(10) 1:3 for interpolator input and 1:4 (max 1:8) for AGC loop

5.2 POLE LENGTH COMPENSATION

Pole width/lengths are programmable by Timken. Available width range from 0.8mm to 4mm.

5.3 AMPLITUDE DETECTION

For Alarm Level and Air Gap detection, an amplitude signal is derived from the analog Hall signals. This signal is also used as control signal for the Automatic Gain Control block which extends the operating air gap range and signal to noise ratio.

5.4 INTERPOLATOR

The analog Hall signals are converted to a digital signal independent to the input amplitude. The non-linear interpolation divides the magnetic input period in up to 160 absolute steps. Hence 4 steps are used for one quadrature output sequence. 40 pulses / period are possible. Additional to this decimal output mode, and for compatibility reasons to the MPS160 (MPS32X) device, a binary output mode (32 pulses / period) is also programmable. Available multipliers are:

zBit	40x	20x	10x	5x	32x	16x	8x	4x

Table 5.2 Possible Interpolation Factors

Parameter	Symbol	Min	Typ	Max	Unit	Note
Interpolation Factor		4/5		32/40		
Absolute Resolution	RES	128/160		128/160	Steps	
Accuracy	SNL		2	3.5	LSB	
Digital Hysteresis	HYS_{DIG}		1 or 2		LSB	Programmable as 1 or 2 bits
Analog Hysteresis	HYS_{ANA}			1	LSB	

Table 5.3 Interpolator Parameters

5.5 REFERENCE PULSE GENERATION

Two different reference pulses C and D can be generated on the same CD pin, (to generate one or more marker pulses that indicate an absolute position). The C pulse is triggered by the phase shift change singularity of the second magnetic track and it occurs at a N to S transition and a D pulse occurs at the S to N transition. The C and D pulses are synchronized according to the figures below. These pulses are programmed by Timken are require the use of a special magnetizing pattern magnetized by Timken. Pulses can be created as much as once per magnetic pole pair for both the C and D pulses.

The whole RP track circuitry can be disabled by programming. The CD pin is in tristate (high impedance output) when the RP track is disabled.

The reference pulse as well as the high resolution track have common mode field rejection within the given tolerance limits.

5.6 INCREMENTAL QUADRATURE A / B AND REFERENCE C / D OUTPUTS

Depending on the interpolation factor, the width of the reference pulses changes relative to the A / B output.

Gain Factor	40x	20x	10x	5x	32x	16x	8x	4x
Phase Width [°]	90	90	45	22.5	90	90	45	22.5
Magnetic [°]	2.25	4.5	4.5	4.5	2.8125	5.625	5.625	5.625
Interpolator [steps]	1	2	2	2	1	2	2	2

Table 5.4 Reference Pulses Width

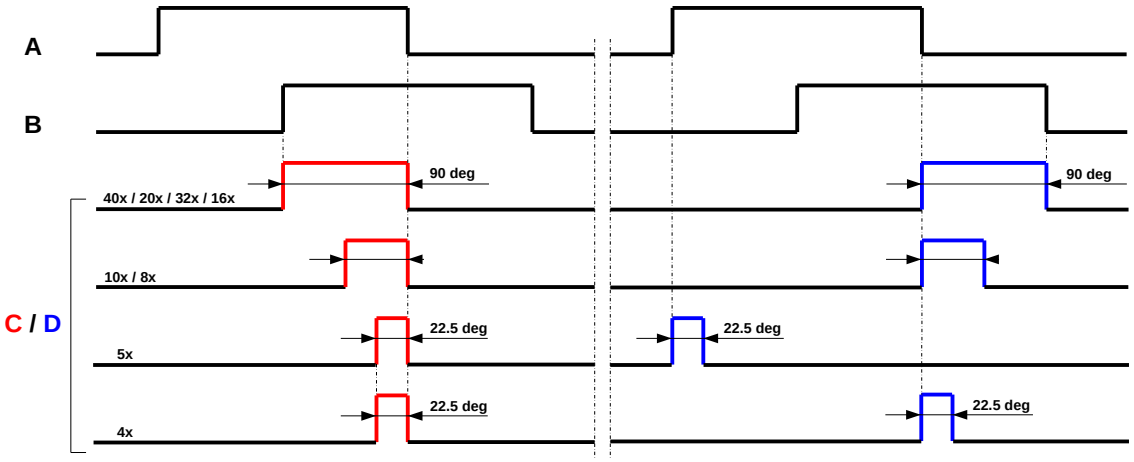


Figure 5.2 C / D outputs with different Interpolation Factors

5.7 LOW POWER MODE

Target of this mode is to reduce the long time power consumption of the device for battery powered applications, without losing pulses. Low Power Mode is activated with the Power Down pin (PD_W) (W input cannot be used in this mode). This mode is enabled by programming at Timken. Only the critical and power consuming elements are kept awake during this mode. All others are powered down.

Due to noise after power up a ±1 step variation can happen at A and B output, even if the magnet is still. In this case the digital hysteresis can be enabled to prevent the output from toggling.

The maximum estimated wake-up time is 100 µs.

The low power mode is activated only when the input signal frequency is very slow (approx 200 Hz). If the PD signal is applied when the input frequency is higher the device will not go in low power mode.

Parameter	Symbol	Min	Typ	Max	Unit	Note
Power Down Current	I_{DD_PD}		2	3	mA	

Table 5.5 Power Down Current

5.8 SELF DIAGNOSTIC

For safety critical applications, signal failures can be indicated over a digital on/off signal on the CAO pin when programmed properly by Timken. The alarm state is activated if one or both of the following situations happen:

The input signal of the interpolator is out of the valid range indicating the air gap is out of range.

The tracking interpolator looses the locked state

The CAO pin will source or sink 5mA and is current limited to 39mA for short circuit protection.

The alarm signal is also available over the quadrature line when programmed by Timken for this function. In this case when an alarm condition occurs an error code of 0 0 1 can be switched to A B CD quadrature pins.

5.9 SPZ PROM

There are 44 permanently programmable bits available for programming by Timken for each specific application. The bits which typically have an impact on each application are:

- Pole width/length selection.
- Open Drain or Push-pull mode outputs
- Resolution Multiplication factors
- Alarm on/off
- Reference channel on/off
- C and or D pulses available on the reference channel.
- 1 or 2 bits of hysteresis.
- W/PD pin used as power down or as W digital input.

5.10 SYNCHRONOUS SERIAL INTERFACE (SSI)

For absolute information readout, a simple Synchronous Serial Interface is implemented.

The device activates the interface with Chip Select (CSn) low. After the time $t_{DO\ acrive}$, Data Out (DO) will change from high impedance (tri-state) to logic high and the read-out will be initiated. After a minimum time t_{CLK_FE}, data is latched into the output shift register with the first falling edge of CLK. Each subsequent rising CLK edge shifts out one bit of data.

A successive measurement is initiated by a high pulse at CSn, with a minimum duration of t_{CSn}.

8 data bits, together with 8 status bits, form a 16 bits output word which is available at the DO pin. This bus pin is tri-state if CSn is high.

Bits D<7:0> represent the measured angular data (absolute position of the magnet relative to the chip). The most significant bit is clocked out first.

Bits S<7:0> represent the status register (system information):

S7	S6	S5	S4	S3	S2	S1	S0
Amplitude Alarm	Interpolator Unlocked Alarm	External digital signal at X pin	External digital signal at PD_W pin	External digital signal at V pin	External digital signal at U pin	REF_sync Signal	Odd Parity bit for transmission safety

Table 5.6 SSI Status Register

The REF_sync is the digital comparator output of the REF channel synchronized to the digital system clock. Together with the absolute angular position information D<7:0> it allows to derive also the C and D pulse generation.

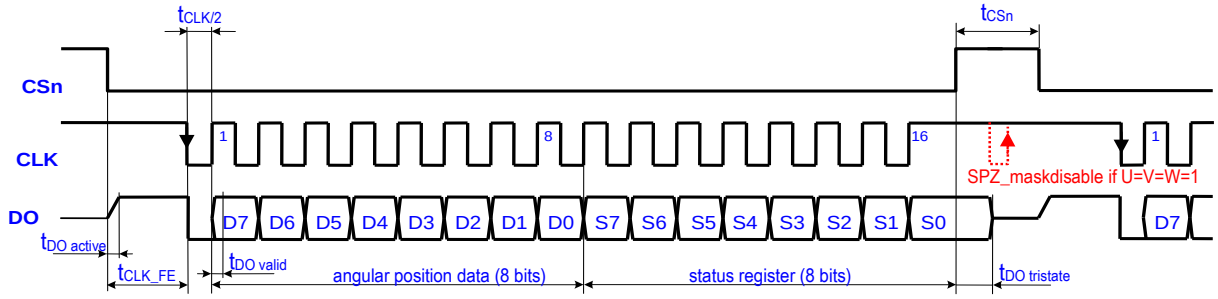


Figure 5.3 SSI Waveforms

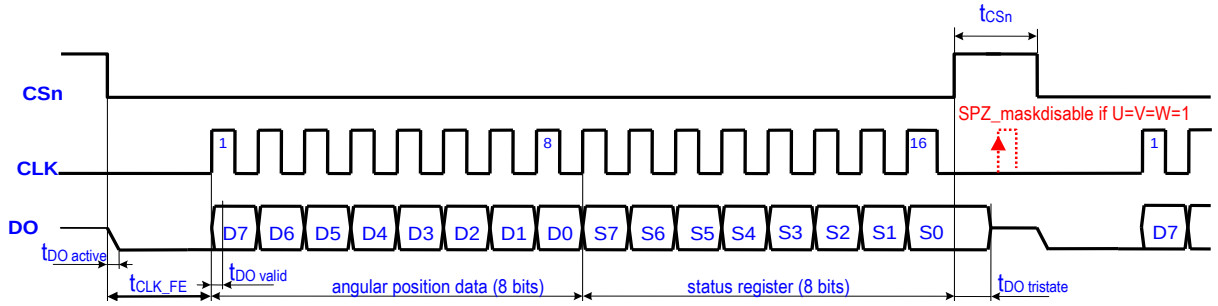


Figure 5.4 SPI Waveforms

Parameter	Symbol	Min	Typ	Max	Unit	Note
Data Output Activated	$t_{DO\ active}$			100	ns	
First Data Shifted to Output Register.	$t_{CLK\ FE}$	750			ns	
Start of Data Output	$t_{CLK/2}$	500			ns	
Data Output Valid	$t_{DO\ valid}$	500			ns	
Data Output Tristate	$t_{DO\ tristate}$			100	ns	
Pulse Width of CSn	t_{CSn}	500			ns	
Read-Out Frequency	f_{CLK}	> 0		1	MHz	

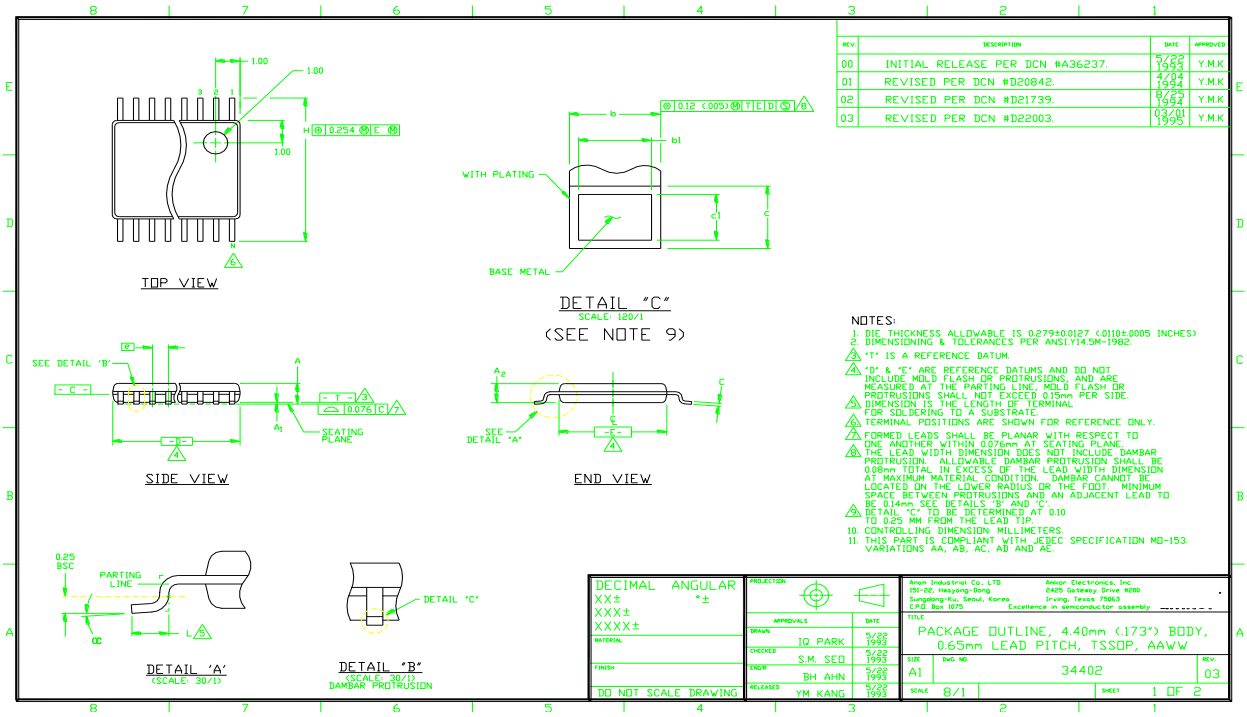
Table 5.7 Estimation of SSI Timing Characteristics

5.11 U / V / W / X EXTERNAL DIGITAL SIGNALS ACQUISITION

Four external digital signals U, V , PD_W and X can be connected to the digital schmitt trigger input pins 24, 23, 14 and 11. The logic state will be written into the SSI Status Register. Input characteristics are defined in Table 3.5.

Rise time (min): 100 ns Fall time (min): 40 ns Pulse width (min): 200 µs

6. PACKAGE-OUTLINE



THIS TABLE IN MILLIMETERS

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	——	——	1.10		AA	2.90	3.00	3.10	8
A_1	0.05	0.10	0.15		AB	4.90	5.00	5.10	14
A_2	0.85	0.90	0.95		AC	4.90	5.00	5.10	16
b	0.19	–	0.30	8	AD	6.40	6.50	6.60	20
b1	0.19	0.22	0.25		AE	7.70	7.80	7.90	24
c	0.090	–	0.20		AF	9.60	9.70	9.80	28
c1	0.090	0.127	0.135						
D	SEE VARIATIONS			4					
E	4.30	4.40	4.50	4					
e	0.65 BSC								
H	6.25	6.40	6.50						
L	0.50	0.60	0.70	5					
N	SEE VARIATIONS			6					
θ	0°	4°	8°						

THIS TABLE IN INCHES

SYMBOL	COMMON DIMENSIONS MIN.	NOM.	MAX.	NOTE	VARIATIONS	D MIN.	D NOM.	D MAX.	N
A	——	——	.0433		AA	.114	.118	.122	8
A_1	.002	.004	.006		AB	.193	.197	.201	14
A_2	.0335	.0354	.0374		AC	.193	.197	.201	16
b	.0075	–	.0118	8	AD	.252	.256	.260	20
b1	.0075	.0087	.0098		AE	.303	.307	.311	24
c	.0035	–	.0079		AF	.378	.382	.386	28
c1	.0035	.0050	.0053						
D	SEE VARIATIONS			4					
E	.169	.173	.177	4					
e	.0256 BSC								
H	.246	.252	.256						
L	.020	.024	.028	5					
N	SEE VARIATIONS			6					
θ	0°	4°	8°						

VARIATION AF IS DESIGNED BUT NOT TOOLED

TITLE
PACKAGE OUTLINE, 4.40mm (.173") BODY,
0.65mm LEAD PITCH, TSSOP, AAWW
SIZE A1 DWG NO. 34402 REV. 03
SCALE 8/1 SHEET 2 OF 2