TIMKEN

MPS512i
Multiplying Encoder ASIC

EXECUTABLE SPECIFICATION

Revision 2.04

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The Timken Company

AEC-Q100 Capable

RoHS Compliant

Protected by US and Foreign Patents

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1. PROJECT SUMMARY

1.1 PURPOSE OF SPECIFICATION

The purpose of this specification is to define the mechanical, environmental and electrical characteristics for MPS512i ASIC sensor.

1.2 ABBREVIATIONS

ASIC -- Application-specific integrated circuit;

HR – High Resolution: also refer to high resolution track of magnetic target wheel, as well as hall sensors and associated circuits or function blocks used to detect and processing the signals;

RP – Reference Pole: also refer to reference track of magnetic target wheel, as well as hall sensors and associated circuits or function blocks used to detect and processing the signals.

ABS – Absolute: also refer to absolute position detection, absolute position signal.

TBD – To Be Determined.

POR – Power-on Reset.

LSB – Least significant bit.

CW – Clockwise direction.

CCW – Counter clockwise direction.

2. BLOCK DIAGRAM

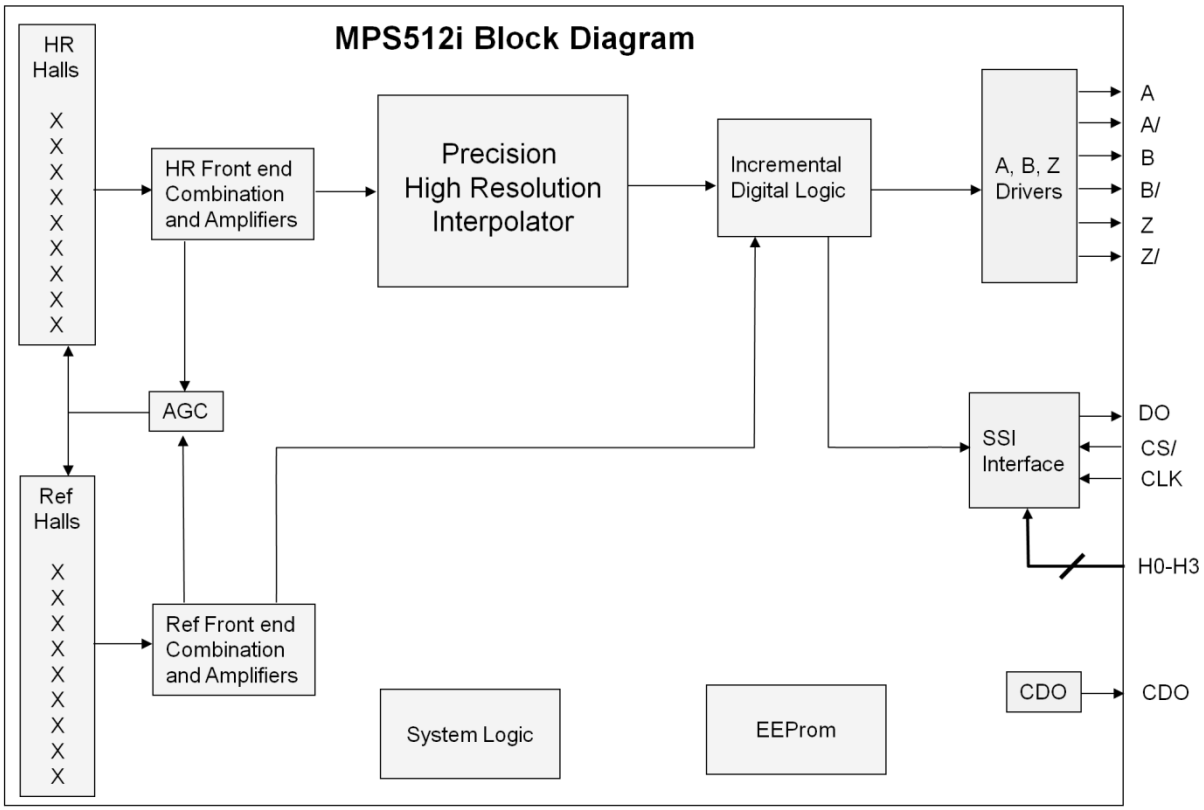

Figure 2.1: MPS512i Block Diagram

3. PIN DESCRIPTION

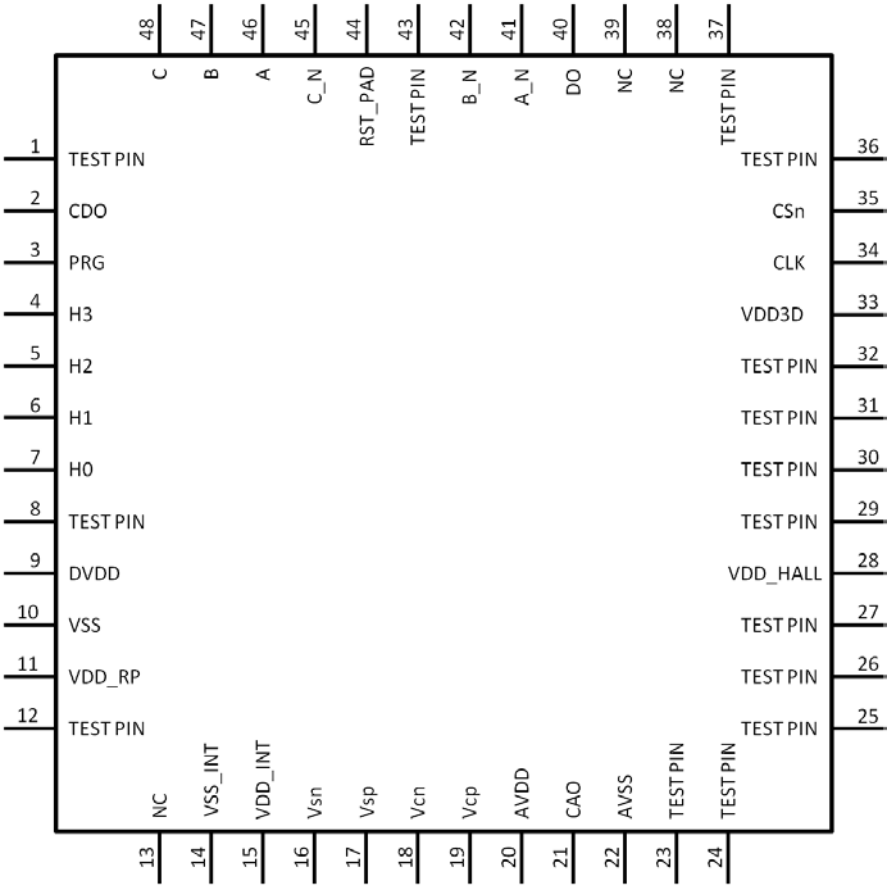

Figure 3.1: Pin Diagram

Table 3.1: Pin Descriptions

Pin #	Pin Name	Pin Type	Special Requirements	Description
1	TEST PIN	NA	Ground to AVSS	Test pin[1]
2	CDO	DO	No Connection if not used	Common Logic Output for internal signals[1]. Can be programmed to output weak magnetic field alarm signal.
3	PRG	NA	Ground to VSS during use	Timken programming pin[1]
4	H3	DI_ST_PD	If not used may be not connected, but in high noise application recommended connect to VSS.	H3 digital input[2]
5	H2	DI_ST_PD	If not used may be not connected, but in high noise application recommended connect to VSS.	H2 digital input[2]
6	H1	DI_ST_PD	If not used may be not connected, but in high noise application recommended connect to VSS.	H1 digital input[2]

Pin #	Pin Name	Pin Type	Special Requirements	Description
7	H0	DI_ST_PD	If not used may be not connected, but in high noise application recommended connect to VSS.	H0 digital input[2]
8	TEST PIN	DI_ST_PD	Connect to VSS.	Test pin[1]
9	DVDD	S	+5V Power. Use decoupling capacitor.	Digital Circuit Supply Voltage
10	VSS	S	Ground	Negative Supply Voltage
11	VDD_RP	S	+5V Power. Use decoupling capacitor.	RP Array Hall Bias Supply Voltage. (Analog circuit power supply)
12	TEST PIN	S	Ground to AVSS during use	Test pin[1]
14	VSS_INT	S	Ground to AVSS during use	HR_INTERPOLATOR ground
15	VDD_INT	S	+5V Power. Use separate decoupling capacitor	HR_INTERPOLATOR power supply
16	VSn	AIO	Ground to AVSS during use	Test pin[1]
17	VSp	AIO	Ground to AVSS during use	Test pin[1]
18	VCn	AIO	Ground to AVSS during use	Test pin[1]
19	VCp	AIO	Ground to AVSS during use	Test pin[1]
20	AVDD	S	+5V Power. Use decoupling capacitor	Positive Analog Supply
21	CAO	AO	No Connection if not used.	Common Analog Output for internal signals. Can be programmed to output one of VSp, VSn, VCp or VCn[1]
22	AVSS	S	Ground	Negative Analog Supply
23	TEST PIN	S	Connect to VSS	Test pin[1]
24	TEST PIN	NA	Ground to AVSS	Test pin[1]
25	TEST PIN	S	Ground to AVSS	Test pin[1]
26	TEST PIN	NA	Ground to AVSS	Test pin[1]
27	TEST PIN	OD	No Connection.	Test pin[1]
28	VDD_HALL	S	+5V Power. Use decoupling capacitor	HR Array Hall Bias Supply Voltage
29	TEST PIN	DO	No Connection	Test pin[1]
30	TEST PIN	NA	Ground to AVSS during use	Test pin[1]
31	TEST PIN	DO	No Connection	Test pin[1]
32	TEST PIN	DO	No Connection	Test pin[1]
33	VDD3V	S	Connect to DVDD if 5V only operation	Digital Supply Voltage. 5V/3.3 V support
34	CLK	DI_ST_PU		SSI Clock input
35	CSn	DI_ST_PU		Chip Select / active low
36	TEST PIN	NA	Ground to AVSS	Test pin[1]
37	TEST PIN	DI_ST_PD	Ground to VSS	Test pin[1]
40	DO	DO		Data Output for SSI
41	A_N/SDA	BI-OD		Incremental quadrature position output A, inverse / Programming Interface Data Line[1]

Pin #	Pin Name	Pin Type	Special Requirements	Description
42	B_N/SCL	BI-OD		Incremental quadrature position output B, inverse / Programming Interface Clock Line[1]
43	TEST PIN	DI_ST_PD	Ground to VSS	Test pin[1]
44	RES_PAD	DI_ST_PU	Connect to +5V during use[3]	Reset pad
45	C_N	DO_OD		Incremental Reference Position Outputs C, inverse
46	A	DO_OD		Incremental quadrature position output A
47	B	DO_OD		Incremental quadrature position output B
48	C	DO_OD		Incremental Reference Position Outputs C

[1] For Timken use only.

[2] The logic status can be captured using SSI. For instance, an external hall switch output can be connected to this input port to enable customer to acquire the hall switch status. There are total 4 available.

[3] If RESET function used, 10k Ohm pull-up resistor recommended.

PIN Types:		
	S	supply pad
	AIO	analog I/O
	AO	analog output
	DI	digital input
	DI_PD	digital input with pull down structure
	DI_PU	digital input with pull up structure
	DI_ST	digital input with schmitt trigger
	DI_ST_PD	digital input with schmitt trigger and pull down structure
	DI_ST_PU	digital input with schmitt trigger and pull up structure
	DO	digital output
	DO_OD	digital output open drain / push - pull
	NC	Not Connected
	OD	Open drain
	BI_OD	Bidirectional/open-drain

Decoupling Capacitors: Four decoupling capacitors are required: 0.1uF on the power pins to Vss. VDDINT should have its own capacitor.

4. GENERAL DEVICE SPECIFICATIONS

4.1 ABSOLUTE MAXIMUM RATINGS (NON OPERATING)

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only. Functional operation of the device at these or any other conditions beyond those indicated under "Operating Conditions" is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 4.1: Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit	Note
Analog Supply Voltage	AVDD	-0.3	7	V	
Digital Supply Voltage	DVDD				
Input Pin Voltage	V_{in}	VSS – 0.5	VDD + 0.5	V	
Input Current (latchup immunity)	I_{scr}	-100	100	mA	Norm: Jedec 17
Electrostatic Discharge	ESD		± 2	kV	Norm: MIL 883 E method 3015
Pkg. Thermal Resistance	Θ_{JA}		58.3	°C / W	Multi-Layer PCB [4]
Pkg. Thermal Resistance	Θ_{JA-EP}		38	°C / W	Multi-Layer PCB [4]
Storage Temperature	T_{strg}	-55	175	°C	According package
Package body temperature	T_{body}		260	°C	Norm: IPC/JEDEC J-STD-020C [1] [2]
Junction temperature	T_J	– 55	150	°C	
Humidity non-condensing		5	85	%	

[1] The reflow peak soldering temperature (body temperature) is specified according IPC/JEDEC J-STD-020C "Moisture/Reflow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices".
[2] The lead finish for Pb-free leaded packages is "Matte Tin" (100% Sn).
[3] The detail subject to change based on the process (technology/manufacture) selection.
[4] & [5] Preliminary

4.2 OPERATING CONDITIONS

All in this specification defined tolerances of parameters are assured over the whole operation conditions range and also over lifetime.

Table 4.1: Operating Conditions

Parameter	Symbol	Min	Max	Unit	Note
Positive Analog Supply Voltage	AVDD	4.5	5.5	V	
Positive Digital Supply Voltage	DVDD				
Positive Digital Supply Voltage	DVDD3	3.0	5.5	V	
Negative Supply Voltage	VSS	0.0	0.0	V	
Power supply current for incremental mode	I_{DDI}		41-90	mA	[3]
Power supply current for ABS mode	I_{DDA}		50-120	mA	Preliminary
Power supply current for independent halls	I_{DDS}		3	mA	Preliminary
Ambient temperature	T_{amb}	– 40	125	°C	[1][4]
Junction temperature	T_J	t.b.d	t.b.d	°C	[1]
EEPROM temperature range	T_{ER}	– 40	125	°C	[5]
	T_{EW}	– 40	125	°C	Erase/Write mode [5]
I/O standard cell temperature range	T_{IO}	– 40	125	°C	
Digital Standard Cell Core Library temperature range	T_{SC}	– 40	125	°C	

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[1] Final value TBD after testing.
[3] All output unloaded, depend of configuration and magnetic field strength
[4] Preliminary
[5] Preliminary

4.3 SYSTEM TIMING PARAMETERS

Table 4.3: System Parameters VDD = 4.5 V

Parameter	Symbol	Min	TYPE	Max	Unit	Note
Power Up Time	$T_{PwrUpABS}$			500	µs	
Power Up Time	$T_{PwrUpInc}$			< $T_{PwrUpABS}$	µs	
Power Up Time	$T_{PwrUpUVW}$			700	µs	
Propagation Delay	T_{prop}			20	µs	[1]

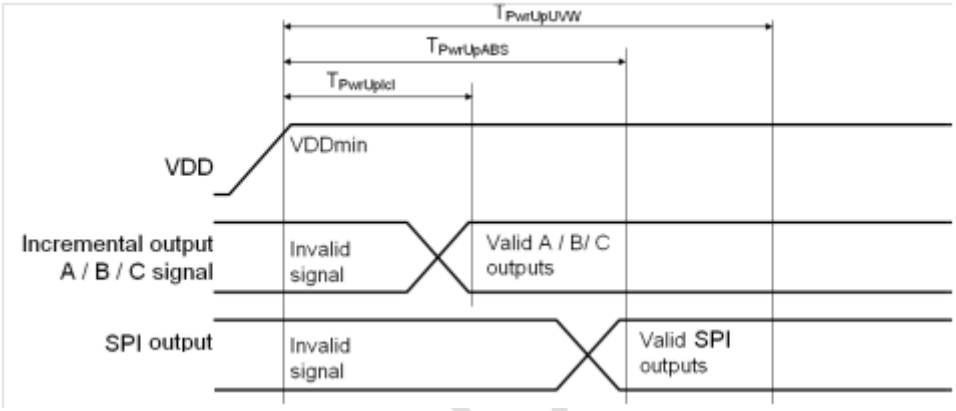

Figure 4.1: Power-on Reset timing.

4.4 DC/AC CHARACTERISTICS FOR DIGITAL INPUTS AND OUTPUTS

4.4.1 Digital Open Drain, Push/Pull Output

Open Drain Mode can be enabled by programming bit (OD). Default: Push Pull Mode.

Table 4.2: A / B / C Open Drain Output .

Parameter	Symbol	Min	Typ	Max	Unit	Note
High level output voltage	V_{OH}	0.8 DVDD			V	
Low level output voltage	V_{OL}			0.4	V	
Current source capability		8			mA	Push/Pull mode
Current sink capability	I_L	10			mA	
Short Circuit Limitation Current	I_{short}			28	mA	
Capacitive load	C_L		40		pF	
Resistive load	R_L		820		Ω	
Rise time	t_R		30		ns	[1]
Fall time	t_F		30		ns	[1]

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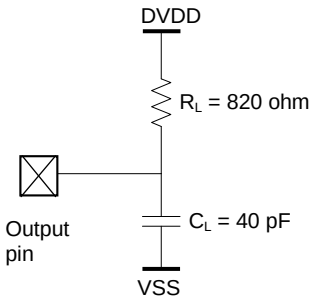

Figure 4.2: Open Drain output load conditions for AC measurement

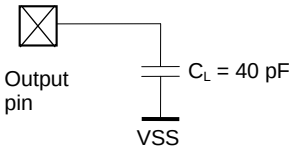

Figure 4.3: Push Pull output load conditions for AC measurement

[1] Transition time between 10% of V_{OH} and 90 % V_{OH}.

4.4.2 Digital input

Table 4.3*:* Schmitt trigger input data (5V).

Parameter	Symbol	Min	Max	Unit	Note
Negative-Going Threshold	V_{t-}	-	-	V	VDD=4.5V
		1.0	-	V	VDD=5.0V
Positive-Going Threshold	V_{t+}	-	-	V	VDD=4.5V
		-	4.0	V	VDD=5.0V

[1]

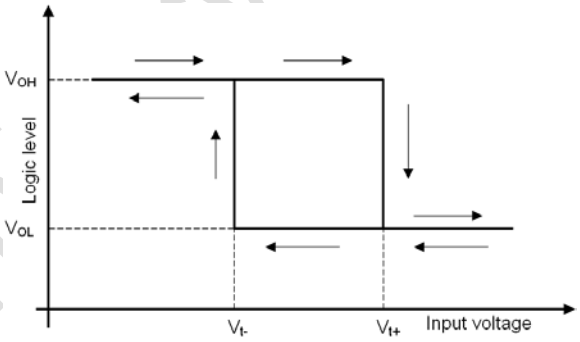

Figure 4.4: Hysteresis of Schmitt trigger input

[1] DetailsTBD: The values for Schmitt trigger cells are only valid for 5V Schmitt trigger cells in the 5V range for supply and input signals.

4.4.3 DO Digital output

Table 4.4: Digital output levels. 4mA tri-state digital output (5V).

Parameter	Symbol	Min	Typ	Max	Unit	Note
Output-low voltage	V_{OL}			0.4	V	VDD=5.5V
Output-high voltage	V_{OH}	4.0			V	VDD=4.5V [1]
Current capability	I_{OUT}			4	mA	Sink and source

[1] maximum high level output voltage = 0.8*DVDD.

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4.4.5 Input and output 3.3 V operation

The ASIC is designed to allow also interface with DVDD3 = 3.3 V devices. In this case pin VDD3V need to connect to 3.3V supply.

Output: A, B, C, A_N, B_N, C_N, DO, U, U_N, W.

Input: CLK, CSn, DI, H0, H1, H2, H3

Table 4.7: 3.3V input/output voltage levels [1]

Parameter	Symbol	Min	Typ	Max	Unit	Note
High level output voltage	V_{OH}	0.8 x DVDD3			V	10 mA
Low level output voltage	V_{OL}			0.4	V	10 mA
High level input voltage	V_{IH}			2.0	V	
Low level input voltage	VI_H	0.8			V	
Negative-Going Threshold	V_{t-}	0.9		1.3	V	
Positive-Going Threshold	V_{t+}	1.5		1.98	V	
Rise time	t_R		30		ns	[1] Preliminary
Fall time	t_F		30		ns	[1] Preliminary

[1] Transition between 10% of V_{OH} and 90 % V_{OH}.

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5. TECHNICAL DESCRIPTION

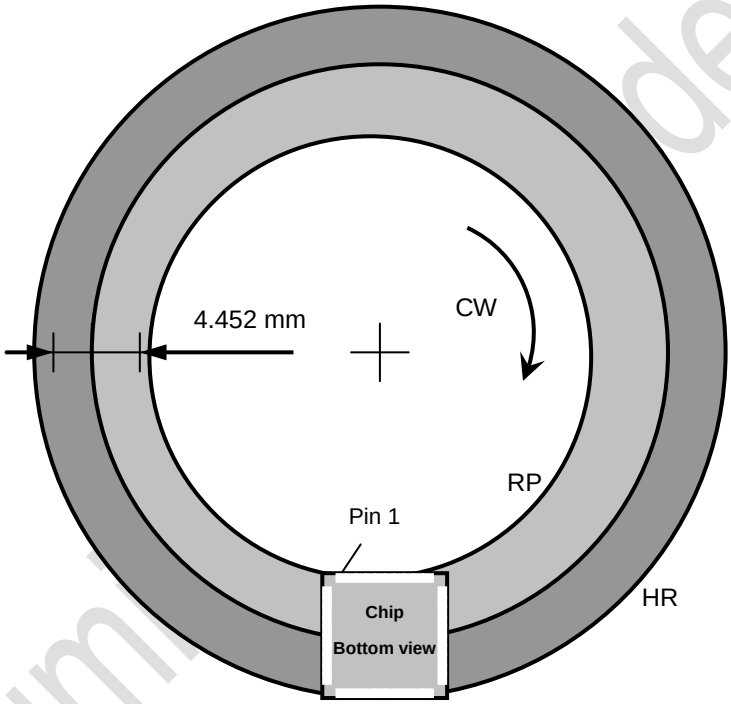
5.1 SHORT DESCRIPTION / KEY FEATURES

MPS512i - The main application of the device is contactless, angular or linear position detection with incremental position signal output. The signal output will be quadrature square waves. Index signal output is synchronized with the incremental position output.

Note on the MPS512 version - The absolute version will provide full or partial (over a portion of a revolution) absolute position. The absolute position signal output can be based on Synchronous Serial Interface or parallel output interfaces. Commutation U, V, W is also provided.

5.2 SYSTEM DIAGRAM / DESCRIPTION

5.2.1 Primary functions for incremental and absolute position detection



RP: Reference track

HR: High resolution track

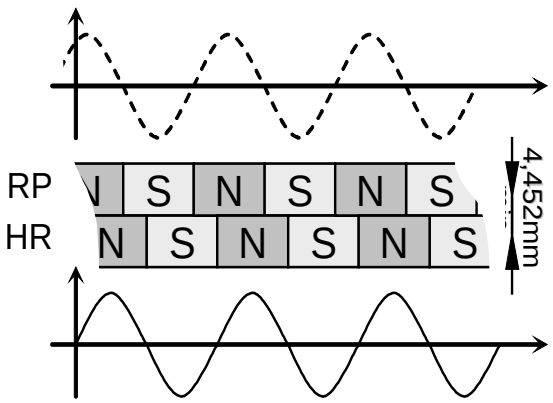


Figure 5.1: System Arrangement Encoder Ring / Sensor ASIC.

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A rotating encoder ring provides the input field by permanent magnetic north (N) and south (S) poles along its circumference. The magnetic field changes alternatively along its circumference. The ASIC Hall sensor system measures the magnetic field and converts it into an electrical signal. One period of sinusoidal waves will be generated by every hall sensor element for every relative displacement of length of every pole-pair in circumferential direction. Front end circuitry amplifies and processes the signals of the sensor elements. As the output of the front end circuitry, a pair of quadrature sinusoidal waves are generated. The quadrature sine wave is fed to the succeeding interpolator circuit. The front end circuitry includes hall sensor signal conditioning, signal amplification and signal processing. The other main functions of the front end circuitry also include sensor offset cancellation, noise reduction, magnetic field offset (magnetic bias field) cancellation.

The exact position of the quadrature sine wave is interpolated linearly by interpolator. Up to 512 digital absolute steps within one pole pair period are first detected. A standard quadrature A / B incremental output is derived to indicate the direction of rotation and to increase the resolution of the encoder ring by a maximum multiplying factor of 128 (pulses/pole pair). The interpolation factor is programmable. The interpolator is high precision and is designed to eliminate the once/cycle counter rollover error associated with many interpolators. (patent pending)

The sensor chip is based on the differential magnetic field so it rejects common mode magnetic fields within the tolerance limits.

When using the quadrature output, a reference signal Z can be enabled, triggered by a magnetic singularity on the second (RP) track of the encoder ring. This allows absolute position measurements over one rotation with quadrature and Z outputs only. Rotation of the magnet until the Z pulse is output is required to obtain absolute position information using this method. See details below on Reference pulse generation.

An Automatic Gain Control (AGC) helps to cover the demanded large dynamic input range. The amplitude of the quadrature sinusoidal waves is calculated and fed into the Automatic Gain Control circuit. The hall element biasing current will be changed based on the detested amplitude. The AGC function can be disabled by the programming. In addition, the amplitude can be output through the diagnosis output Pin CAO. Since the amplitude is dependent on the strength of input magnetic field (less than magnetic field offset), diagnosis information of insufficient magnetic field strength will be available to identify situations such as improper air gap, sensor's out-of-range of target wheel.

The alarms available for the MPS512i are:

- Air gap alarm. This alarm signals air gap out of range
- Interpolator Unlocked Alarm: This alarm signals if the interpolator should get unlocked from tracking the sin/cos waves

Detailed for Reference Pulse generation

A reference pulse Z can be generated on the Z pin, which is used to generate one or more marker pulses that indicate an absolute position. The reference pulse is triggered by the phase shift change singularity of the second (RP) magnetic track compared with the HR track. The phase shift change singularity usually occurs at an N to S transition of HR track. The reference pulse is synchronized to HR signal as well as the incremental quadrature square waves A/B. The generation of phase shift change singularity requires the use of a special magnetizing pattern designed by Timken. Pulses can be created as much as once per magnetic pole pair or over a number of pole pairs.

A second hall element array (RP hall element array) is used detect the second (RP) track magnetic field. For the reference pulse purpose, the number of active hall elements can be reduced in order to minimum power consumption. A configuration of the RP hall element array is shown in Figure 5.2.2. Similar to the front end circuitry of HR hall array, the sensor signal conditioning, amplification circuits are needed to obtain signal from the 4 hall element RP array. Only summation is necessary for the 4 hall elements.

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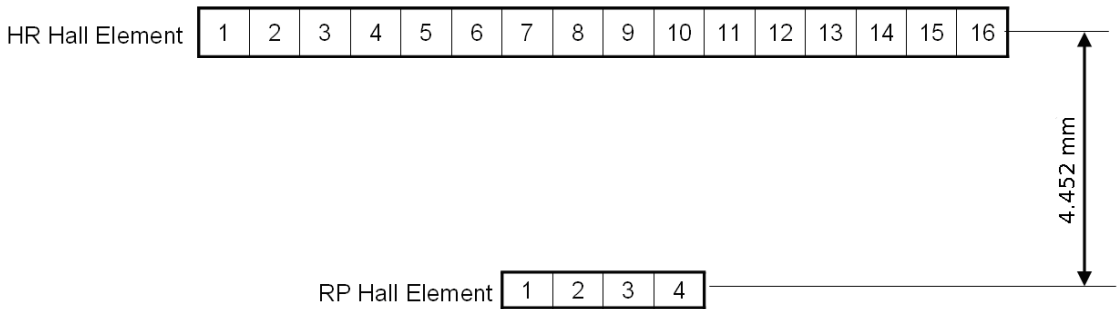

Figure 5.2: Configuration of RP hall element array.

Note: The Rp Halls are near pins 1-12 and the HR Halls are near pins 37-48

The configuration for generating the reference pulse is programmed by Timken. The sensors and whole circuitry associated with RP signal can be disabled by programming settings. The Z pin is in tristate (high impedance output) when the RP function is disabled.

The reference pole track as well as the high resolution track have common mode magnetic field. The ASIC is required common mode magnetic field rejection within the given tolerance limits.

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6. DETAILED SYSTEM AND BLOCK SPECIFICATIONS

6.1 MAGNETIC INPUT

Sinusoidal characteristics of the magnetic Encoder Ring apply to High Resolution (HR) and Reference Pole (RP) Track are shown in Table 6.1.1. [1][2]

Table 6.1: Magnetic Input Characteristic

Parameter	Symbol	Min	Max	Unit	Note
Magnetic Pole Length (Full Period/FP)	$L_{P\text{-}FP}$	1.0	6	mm	[3]
Magnetic Period (Full Period/FP)	$T_{P\text{-}FP}$	2.0	12	mm	$T_{P\text{-}FP} = 2 \times L_{P\text{-}FP}$
Magnetic Pole Length (Half Period/HP)	$L_{P\text{-}HP}$	4.0	8.0	mm	[3]
Magnetic Period (Half Period/HP)	$T_{P\text{-}HP}$	8.0	16.0	mm	$T_{P\text{-}HP} = 2 \times L_{P\text{-}HP}$
Magnetic Pole Length (Double Period/FP)	$L_{P\text{-}DP}$	0.6	1.25	mm	[3]
Magnetic Period (Double Period/FP)	$T_{P\text{-}DP}$	0.75	2.5	mm	$T_{P\text{-}DP} = 2 \times L_{P\text{-}DP}$
Pole Length Relative Accuracy	P		±4	%	
Magnetic Amplitude	A_{mag}	2	60	mT	[4] [5][6][7]
Operating Dynamic Input Range			TBD		[8]
Magnetic Offset	Off_{mag}	± 15	TBD	mT	DP & FP modes
			± 0.5	mT	HP mode [9]
Amplitude Modulation	AM_{mag}		± 15	%	F_{AM_max}
Magnetic Temperature Drift	T_{dmag}		– 0.2	%/K	
Input Frequency	f_{mag}	0	10	kHz	[10]

[1] Hall array configuration mode can be programmed.
[3] $P = (L_P – L_{P,th}) / L_{P,th}$ where $L_{P,th}$ is the theoretical pole length;
[4] Absolute magnetic input minimum 2 mT over all parameters. This minimum input results into a transition noise of 2 LSB_{PP}. An increased hysteresis of 2 LSB must be chosen for no additional pulses, or the input magnetic amplitude must be doubled to 4 mT to use 1 LSB hysteresis.
[5] The magnetic input minimum amplitude increases with increasing pole length

Table 6.2: Min. Magnetic Amplitude vs. Pole Length

Pole Length [mm]	0.6 to 1.25	1.13 to 2.15	1.51 to 2.50	2.50 to 4	4 to 6
Min. Magnetic Amplitude [mT]	2	3	2	3	4
Mode	DP	FPS (12)	FP-A (16) (Normal Operating Mode)	FP-B (16) (Normal Operating Mode)	HP

[6] Due to shock sudden variation of 20% are possible.
[7] The minimum magnetic field of the magnetic singularity can go down to 70% of the minimum magnetic amplitude of the HR track.
[9] No differential signal processing for canceling magnetic offsets on the HR for the signal is possible in HP mode.
[10] Refer to mode change

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6.2 INTERPOLATION FACTOR

Three interpolation modes: binary output mode, decimal output mode and MPS160 compatible mode, are available through a programming bit (BD). The non-linear interpolation divides the magnetic input period in up to 512/400/320 absolute steps. Hence 4 steps are used for one quadrature output sequence. 128/100/80 lines / period are possible.

Available multipliers are:

Table 6.3: Possible Interpolation Factors

Interpolation Factors / Programming bits	Symbol	100x	80x	50x	40x	25x	20x	10x	128X	64X	32x	16x	8x	4x
Binary/Decimal mode	BD	0	0	0	0	0	0	0	1	1	1	1	1	1
Interpolation Factors 0	IF0	1	0	1	0	1	0	1	0	1	0	1	0	1
Interpolation Factors 1	IF1	0	1	1	0	0	1	1	1	1	0	0	1	1
Interpolation Factors 2	IF2	0	0	0	1	1	1	1	0	0	1	1	1	1

The output frequency of counts depends on the interpolation factor and the input frequency.

6.3 DIGITAL HYSTERESIS

programmable by Timken.

Table 6.4: Maximum allowable hysteresis

Interpolation Factors / Programming bits	100x	80x	50x	40x	25x	20x	10x	128X	64X	32x	16x	8x	4x
No. of Hysteresis bits	3	2	2	1	1	1	0	4	2	1	0	0	0
No. of Hysteresis bits (Low input)	6	4	3	2	2	1	1	8	4	2	1	0	0

6.4 PROGRAMMING

The MPS512i is fully programmable by Timken. The key user programmable functions include:

- Pole spacing
- Resolution multiplier
- Reference pulse on/off
- Outputs: Push-pull or open collector
- Hysteresis
- Hall mode: (sets ranges of pole widths)
- Alarms

6.5 SSI OUTPUT

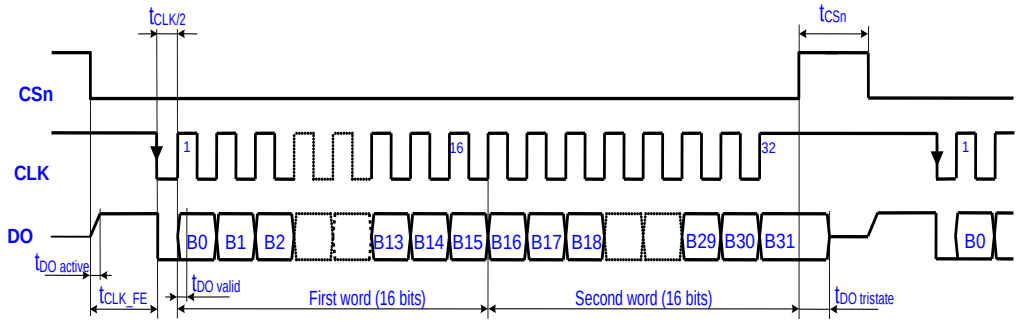

Figure 6.1: SSI Waveforms

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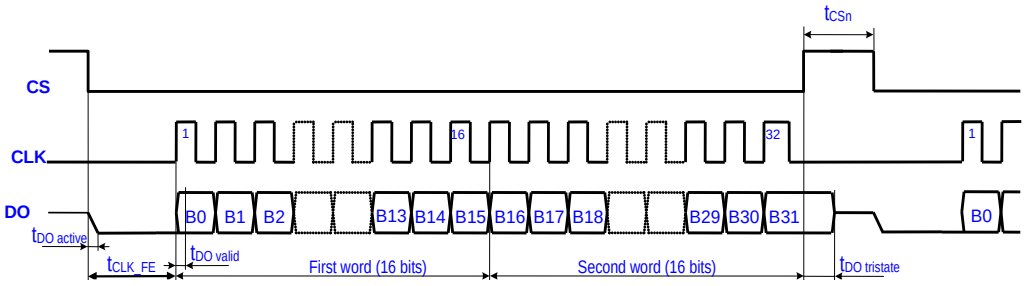

Figure 6.2: SPI Waveforms

Table 6.5: SSI Timing Characteristics

Parameter	Symbol	Min	Typ	Max	Unit	Note
Data Output Activated	$t_{DO\ active}$			100	ns	
First Data Shifted to Output Register.	$t_{CLK\ FE}$	750			ns	
Start of Data Output	$t_{CLK/2}$	500			ns	
Data Output Valid	$t_{DO\ valid}$	500			ns	
Data Output Tristate	$t_{DO\ tristate}$			100	ns	
Pulse Width of CSn	t_{CSn}	500			ns	
Read-Out Frequency	f_{CLK}	> 0		4	MHz	

Table 6.6: SSI - Frame

HR									Pole Pair Counter				S2	S1	S0
D0	D1	D2	D3	D4	D5	D6	D7	D8	PC0	PC1	PC2	PC3	Alarm	Reserved	Even Parity bit
Bit0	Bit1	Bit2	Bit3	Bit4	Bit5	Bit6	Bit7	Bit8	Bit9	Bit10	Bit11	Bit12	Bit13	Bit14	Bit15
PC	H input							S9	S8	S7	S6	S5	S4	S3	S0
PC4	H0	H1	H2	H3	Reserved	Reserved	Reserved	Interpolator Alarm	Air Gap Alarm	Reserved	REF_sync Signal	Reserved	Reserved	Reserved	Even Parity bit
Bit16	Bit17	Bit18	Bit19	Bit20	Bit21	Bit22	Bit23	Bit24	Bit25	Bit26	Bit27	Bit28	Bit29	Bit30	Bit31

Table 6.7: Bit definitions

Bit definitions:	
Bit0 – Bit8:	D8:D0: Interpolator counter data, one pole pair absolute position data, LSB first
Bit9 - Bit12:	D12:D0: the lower 4 bits of pole pair counter, LSB first;
Bit13:	S2:Alarm signal if any of (1) HR interpolator unlock Alarm; (2) Air gap Alarm;

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Bit14:	Reserved
Bit15:	S0:Even Parity bit for Bit0:Bit14
Bit16:	D13:MSB of pole pair counter
Bit17 - Bit20:	H0 :H3: External logic signal at H0 - H3 pins
Bit21 - Bit23:	Reserved
Bit24:	S9: HR Interpolator unlock Alarm
Bit25:	S8: Air gap alarm
Bit26:	Reserved
Bit27:	S6: REF_syn c Signal
Bit28:	S5: CDO
Bit29:	S4: Reserved
Bit30:	S3: Reserved
Bit31:	S0: Even parity bit for Bit16:Bit30

Contact Timken for details.

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7. MARKING / PACKAGE

Package Type	Pkg Size (mm) L x W	PAD Size (mm) L x W	Ex. PAD Size (mm) L x W	Lead Pitch (mm)	Pkg Thickness (mm)	L/F Type	L/F Plating	MSL LEVEL
48L QFN	7.0 x 7.0	5.8 x 5.8	5.55 x 5.55	0.5	0.9	194FH	Ring	

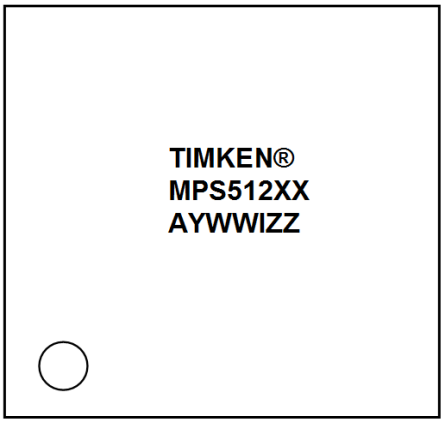

Figure 7.1: Package Marking

Marking:

First Line	TIMKEN®	
Second Line	MPS512XX	XX: version
Third Line	AAAAAAA	Lot / date codes

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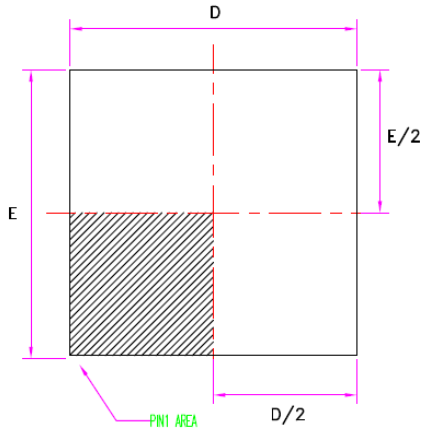
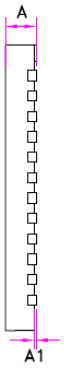
8. PACKAGE-OUTLINE

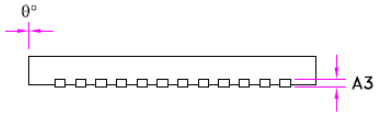
7 X 7 X 0.90MM QLMP

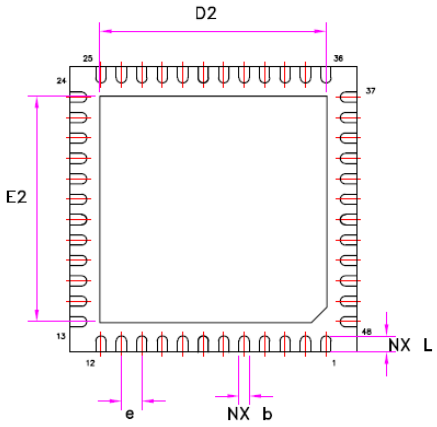
QUAD LEADLESS MOLDED PACKAGE

PACKAGE INFORMATION









JEDEC#	MO-220 / VKKD			
TYPE	48 LEAD			
Dimension	mm		mils	
SYMBOL	Min	Max	Min	Max
A	0.85	0.95	33.46	37.40
A1	0	0.05	0	1.97
A3	0.175	0.225	6.89	8.86
D	6.9	7.1	271.65	279.53
E	6.9	7.1	271.65	279.53
D2	5.5	5.6	216.54	220.47
E2	5.5	5.6	216.54	220.47
e	0.5 BSC		19.69 BSC	
NX b	0.20	0.30	7.87	11.81
NX L	0.35	0.45	13.78	17.72
θ°	0°	4°	0°	4°
ND	12			
NE	12			

NOTES

1. SPADE WIDTH, LEAD WIDTH AND LEAD THICKNESS EXCLUSIVE OF SOLDER PLATE
2. PACKAGE OUTLINE EXCLUSIVE OF MOLD FLASHES AND BURR DIMENSIONS
3. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS. COPLANARITY SHALL NOT EXCEED 0.08mm.
4. WARPAGE SHALL NOT EXCEED 0.10mm.
5. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012.
   DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL#1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.

PREPARED BY	SSH	REF. NO.	REV. NO.
CHECKED BY	XXXX	DIM-QLMP-7X7x0.90	0
APPROVED BY	XXXX		DATE
			12.10.10

Note: Distance from surface of package to Hall sensors is 0.20 to 0.25mm.